



# Intel<sup>®</sup> IXP400 Software Version 2.0

*Software Product Specification*

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*June 2005*



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## Revision History

Date	Revision	Description
June 2005	001	Initial release.

## 1.0 Product Context

Intel® IXP400 Software v2.0 enables the underlying capabilities of the Intel® IXP4XX Product Line of Network Processors.

**Table 1. Intel® IXP400 Software v2.0 Compatibility Reference**

Support Category	Details
Processors supported	<ul style="list-style-type: none"> <li>Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor</li> <li>Intel® IXP45X and Intel® IXP46X Product Line of Network Processors</li> </ul>
Operating system/development environments	<ul style="list-style-type: none"> <li>Wind River* VxWorks* Developer Tool Kit 2.2.1 (Tornado* 2.2.1 / VxWorks 5.5.1) with Gcc compiler [IXDP425 BSP version 1.2/10, IXDP465 BSP version 1.2/0]</li> <li>MontaVista* Linux* Professional Edition 3.1 with Gcc compiler</li> </ul>
Hardware platform support	<ul style="list-style-type: none"> <li>Intel® IXDP425 / IXCDP1100 Development Platform</li> <li>Intel® IXDP465 Development Platform</li> </ul>

## 2.0 Product Specifications

This section presents features supported by software release 2.0:

### ATM Access

- AAL (AAL5, AAL0, OAM)
- Configure and activate up to 12 ports on the UTOPIA level-2 interface
- Up to 32 VC channels supported
- ATM configuration and management component

### ATM Transmit Scheduler

- Maximum number of VCs: Up to 32 on device at any time
- Maximum of 1 nrt-VBR
- No restriction (up to 32) on number of UBR VCs
- Traffic Types: nrt-VBR, UBR
- Maximum of 8 ports and a total of 32 VCs across all ports
- CDVT not supported; CDVT not valuable for CPE devices
- Restriction PCR must be equal to SCR for VBR VC
- PCR for nrt-VBR, UBR
- SCR for nrt-VBR
- MBS for nrt-VBR

### Security

- Silicon Crypto algorithms enabled for use via software:
  - DES (64-bit block, 64-bit key)
  - 3DES (64-bit block, 192-bit key)

- AES (128-bit block, 128/192/256-bit key)
- ARC-4 (8-bit block, 128-bit key)
- Encryption modes of operation:
  - ECB
  - CBC
  - CTR (For AES only)
  - AES-CCM
- Silicon Crypto Authentication algorithms enabled for use via software:
  - Generic (non-HMAC) SHA1 and MD5 hashing
  - HMAC-SHA1 (512-bit block size, from 20- to 64-byte key sizes)
  - HMAC-MD5 (512-bit block size, from 16- to 64-byte key sizes)
  - WEP ICV (32-bit CRC polynomial)

### **DMA**

- DMA capabilities to offload data transfers between peripherals and processor memory
- Transfer modes: Copy only, Copy and Clear Source, Copy and Byte Swap, Copy and Byte Reverse
- Source and Destination Transfer Widths: Burst, 8-bit, 16-bit, 32-bit

### **Ethernet Access**

- Enabled additional MII via NPE-A (for a total of 3) [IXP465 network processor ONLY]
- Provides data, control and management support for Ethernet MAC devices
- Ethernet frame transmission and Reception
- Ethernet MAC statistics, Tracking and Reporting
- Tx and Rx queue support
- IEEE 802.1d-compliant bridge
- Supports Ethernet frames up to 16,320 bytes (jumbo)

#### ***Ethernet Receive Path Services***

- Ethernet receive data transport
- Frame size filtering services
- Ethernet filtering database services
- Destination MAC address filtering
- Destination port identification
  - \* Spanning tree services
    - Spanning tree BPDU identification and delivery
    - Spanning tree port blocking
  - \* Source MAC address learning assistance
  - \* MAC address aging assistance
  - \* VLAN ingress services
    - VLAN ingress acceptable frame type filtering
    - VLAN ingress ID copy
    - VLAN ingress tagging/untagging

- VLAN ingress identification
- VLAN ingress filtering
- Port ID extraction
- \* Firewall services
  - Invalid source MAC address filtering
  - MAC address blocking
  - MAC address admission
- \* IEEE802.3 to IEEE802.11 header conversion
  - IEEE802.3 to IEEE802.11 conversion configuration
  - IEEE802.3 to IEEE802.11 conversion execution
- \* Miscellaneous frame inspection/extraction services
  - Destination and source MAC address copy
  - Frame header type report
- \* Receive QoS services
  - Receive QoS configuration
  - Receive QoS classification and delivery

**Ethernet Transmit Path Services**

- Ethernet transmit data transport
- Transmit QoS service
- Frame size filtering service
- IEEE802.11 to IEEE802.3 header conversion
- VLAN egress services
  - \* VLAN egress filtering
  - \* VLAN egress ID-based tagging/untagging

**Ethernet Database**

- NPE-based MAC address-learning
- Each NPE can managed up to 511 MAC addresses

**Ethernet PHY**

- Provides access to a minimum number of necessary configuration registers on Ethernet PHYs
- MDIO bus scanning for up to 32 available PHYs
- Configure PHY link speed, duplex, and negotiation settings
- Retrieve PHY status and link state
- Supported PHYs
  - Intel® LXT971 Fast Ethernet Transceiver
  - Intel® LXT972 Fast Ethernet Transceiver
  - Intel® LXT973 Fast Ethernet Transceiver
  - Micrel Semiconductor\* / Kendin\* KS8995 5-Port 10/100 switch with PHY

**Note:** Other PHYs may be supported (user-upgradeable)

**Feature Control**

- Processor-specific build mechanism

- Read and or disable Intel® IXP4XX Product Line of Network Processors capabilities
- Enable or disable software features

### **HSS-Access Layer**

- Provides API for T1/E1 and high-speed serial services
- Timeslot Provisioning
  - Static Timeslot provisioning
  - Limit of one multi-timeslot packetized channel per T1/E1
- Channel Processing
  - Bit Inversion on Per-Channel Basis
  - Packetized N x 64Kbps channels from any TDM stream [where  $1 \leq N \leq 32$ ]; a channel may not span multiple T1/E1s
  - Packetized (N x 56Kbps with CAS bit) channels from any TDM stream [where  $1 \leq N \leq 32$ ]; a channel may not span multiple T1/E1s
  - Channelized Service (64 Kbps only)
- Channel Data Processing Services
  - Transparent (Raw) service for Packetized channels without frame alignment
- Basic T1/E1
  - One packetized N x 64 Kbps or N x 56 Kbps Channel per T1/E1, for up to eight T1/E1s
  - Sixty-four non-packetized 64-Kbps Channels, thirty-two channels per HSS port

### **NPE-Downloader**

- Supports facility to download Intel-programmed microcode images to NPEs
  - NPE A Image options
    - \* Ethernet, HSS, ATM, DMA, Crypto
  - NPE B Image options
    - Ethernet, DMA
  - NPE C Image options
    - \* Ethernet, DMA, Crypto

### **NPE Message Handler**

- Responsible for sending messages from software components on the Intel XScale® Core to the NPEs
- Interrupt-Driven or Polled Operation

### **Performance Profiling [IXP42X product line ONLY]**

- Provides access to available performance statistics from the Intel XScale core's PMU, Internal bus PMU and XCycle
- Clock Counting
- Event Counting
- Time-based sampling
- Event-based sampling



- Output to a file support

#### **UART Access**

- Baud rates between 9,600 and 912.6 Kbps
- 16550 UART support
- Independent UART configuration support

#### **USB 1.1 Device Access**

- 16 endpoints
- Half-duplex at a 12-Mbps baud rate, slave only

#### **I<sup>2</sup>C Access**

- I<sup>2</sup>C support [IXP465 ONLY]

#### **SSP Access**

- SSP support [IXP465 ONLY]

#### **Timesync Access**

- TimeSync support used for IEEE1588 [IXP465 ONLY]

#### **Parity Error Notification Access**

- ECC and Parity error detection support [IXP465 ONLY]



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