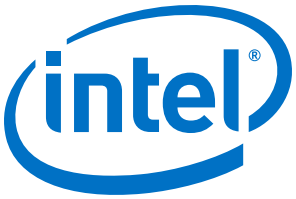

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Contents

1 Arria 10 Transceiver Native PHY IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Quartus Prime Design Suite Update Release Notes*.

Related Links

Quartus Prime Design Suite Update Release Notes

1.1 Arria 10 Transceiver Native PHY IP Core v15.1 Revision History

Table 1. v15.1 November 2015

Description	Impact
Issue: ACDS 15.1 introduces a necessary fix for Arria 10 transceiver designs. This fix introduces a change that affects post-fit simulation for designs containing Arria 10 Transceiver Native PHY, Arria 10 Transceiver ATX PLL, Arria 10 Transceiver CMU PLL, and Arria 10 fPLL IP cores. `pll_powerdown` is not connected for HSSI PLL IPs. **Workaround:** Users requiring post-fit simulation of the transceiver PLLs in ACDS 15.1 need to disable the "Transceiver Reset Sequencer" for their design to produce a post-fit simulation netlist. However, this cannot and should not be used to produce the final bitstream for hardware. Hardware requires the "Transceiver Reset Sequencer" to be enabled. To disable the "Transceiver Reset Sequencer" in the Quartus Prime software, add the following QSF to the Quartus Settings File for the project: `set_global_assignment -name VERILOG_MACRO "ALTERA_XCVR_A10_ENABLE_ANALOG_RESETS=1"` This will completely disable the reset sequencer in the design and restore the old behavior. This method does not allow post-fit simulation of the "Transceiver Reset Sequencer" logic. **Resolution:** A modification to the PLL simulation models is planned for a subsequent release of ACDS 15.1 to remove the reset requirement.	`pll_powerdown` inputs to the Arria 10 Transceiver ATX PLL, Arria 10 Transceiver CMU PLL, and Arria 10 fPLL IP cores for Quartus Prime synthesis. As a result, the resulting generated post-fit simulation will not have a reset input connection for the PLL and post-fit simulation will likely fail.
In Arria 10 devices, you may observe marginal core-to-periphery and periphery-to-core setup and hold violations (range: 80 ps - 100 ps) in transceiver based designs. You can ignore these violations in the 15.1 release.	These setup and hold violations have no impact on hardware designs.
The Arria 10 Transceiver Native PHY IP core adds logic that controls and sequences the assertion and deassertion of the `rx_analogreset` and `tx_analogreset` signals internal to the core. The logic that performs this sequencing is inserted by the Quartus Prime software during synthesis.	This change requires you to make one of two changes to your reset control logic that drives the `rx_analogreset`, `tx_analogreset`, and `tx_digitalreset` signals. Refer to the *Resetting Transceiver Channels* chapter of the *Arria 10 Transceiver PHY User Guide*

continued...

Description	Impact
	for details about the new reset sequence requirements.
A new option in the Native PHY IP core called "Include PMA analog settings in configuration files" allows you to select whether you want analog settings and their dependent parameters to be part of your configuration files (MIF, SV, or H) for dynamic reconfiguration. If you select this option, a new tab opens up for you to select various analog settings.	You must still use Quartus II Settings File (**.qsf**) assignments to specify the analog settings for their current configuration in the Quartus Prime software. This new GUI option does not remove the requirement to specify **.qsf** assignments for their analog settings. This option only allows you to include analog settings as part of the configuration files for reconfiguration.

1.2 Arria 10 Transceiver Native PHY IP Core v15.0 Revision History

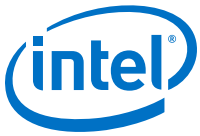
Table 2. 15.0 May 2015

Description	Impact
Changed bit settings.	You must upgrade any IPs generated prior to Quartus II software v15.0.
Added the following warning message to the GUI: "**Enable dynamic reconfiguration** should be enabled when **Enable datapath and interface reconfiguration** is enabled". This message appears when dynamic reconfiguration is disabled while datapath reconfiguration is enabled.	-
Updated tooltips and added information messages for the parameters in the table below *Note:* Information messages are displayed only if the parameter is enabled.	-

Table 3. Tool Tip and Information Message Updates

Parameter	Tool Tip Update	Information Message
`tx_pma_clkout`	Enables the optional `tx_pma_clkout` output clock. This is the parallel clock from the TX PMA. This port is not to be used to clock the data interface.	The `tx_pma_clkout` port is not to be used to clock the data interface.
`rx_pma_clkout`	Enables the optional `rx_pma_clkout` output clock. This is the recovered parallel clock from the RX CDR. This port is not to be used to clock the data interface.	The `rx_pma_clkout` port is not to be used to clock the data interface.
`tx_pma_div_clkout`	Enables the optional `tx_pma_div_clkout` output clock. This port	The `tx_pma_div_clkout` port should not be used for register mode data transfers.

continued...



Description			Impact
Parameter	**Tool Tip Update**	**Information Message**	
	should not be used for register mode data transfers.		
`rx_pma_div_clkout`	Enables the optional `rx_pma_div_clkout` output clock. This port should not be used for register mode data transfers.	The `rx_pma_div_clkout` port should not be used for register mode data transfers.	
Added the following information message to the GUI for `tx_std_bitslipboundarysel`: "The `tx_std_bitslipboundarysel` port must be enabled if Standard PCS TX bitslip capability is desired." This message is displayed if TX bitslip is enabled and Std PCS is used.			-
Added warning messages for merging simplex IPs. The messages are displayed conditionally. For example, when embedded debug is enabled in a simplex design. The following are example messages: • If this TX Simplex Native PHY instance needs to be merged with an RX Simplex Native PHY instance or a CDR PLL IP instance, ensure that reconfiguration inputs of both the PHY instances are driven by the same source. • If this RX Simplex Native PHY instance needs to be merged with an TX Simplex Native PHY instance, ensure that reconfiguration inputs of both the PHY instances are driven by the same source. • This TX Simplex Native PHY instance cannot be merged with an RX Simplex Native PHY instance or a CDR PLL IP instance. • This RX Simplex Native PHY instance cannot be merged with a TX Simplex Native PHY instance.			-
Removed the **triggered** option from the **DFE adaptation mode** parameter. If an IP core is generated before 15.0 with the **triggered** option selected for **DFE adaptation mode**, automatic upgrade maps **triggered** to **continuous**. Also updated the tool tip for **DFE adaptation mode** accordingly.			-
Added options to enable/disable the `tx_pma_iqtxrx_clkout` and `rx_pma_iqtxrx_clkout` ports. The ports are targeted for cascading the RX/TX PMA output clocks to the input of a PLL.			-
Fixed the issue where the following parameter values were not setting properly if using Riveria: • `hssi_10g_tx_pcs_pseudo_seed_a` • `hssi_10g_tx_pcs_pseudo_seed_b` • `hssi_8g_rx_pcs_wa_pd_data` • `pma_tx_buf_xtx_path_pma_tx_divclk_hz` • `pma_rx_buf_xrx_path_pma_rx_divclk_hz` • `pma_tx_buf_xtx_path_tx_pll_clk_hz`			-
When generating configuration files for RX-only configurations, the PHY incorrectly includes registers related to the TX CGB block. When generating configuration files for TX-only configurations, the PHY incorrectly includes registers related to the RX PMA adaptation blocks.			The RX/TX configuration file inadvertently contains configuration data for the complimentary simplex direction. This causes an issue when a TX and RX PHY are merged to the same location because streaming the configuration data to one side affects the other.

Description	Impact
	Embedded streamer configurations are not affected as such and are not permitted in simplex configurations.

1.3 Arria 10 Transceiver Native PHY IP Core v14.1 Revision History

Table 4. 14.1 December 2014

Description	Impact
Added support for multiple silicon revisions supported for ACDS 14.1 version of the Quartus II software.	-
Added a new parameter for Interlaken protocol implementation called **Enable Interlaken TX random disparity bit**. When enabled, a random number is used as a disparity bit.	
Changed the option "Manual (PLD controlled)" to "Manual (FPGA fabric controlled)" for the **RX word aligner mode** parameter.	-
Changed the option "SATA" to "SATA/SAS" for **PMA configuration rules** parameter.	-
Changed the descriptions of parameters **CTLE adaptation mode** and **DFE adaptation mode**.	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

1.4 Arria 10 Transceiver Native PHY IP Core v14.0 Revision History

Table 5. v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for PCS-Direct mode. The PCS-Direct mode enables you to bypass all the internal PCS blocks.	-
Changed the maximum data rate supported by GT channels to 28300 Mbps.	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the **Dynamic Reconfiguration** tab.	-
Changed **Enable embedded JTAG AVMM Master** parameter to **Enable Altera Debug Master Endpoint** parameter.	-
Added the following parameters: • **PMA Configuration Rules**. • **Enable fast sync status reporting for deterministic latency SM** under the **Word Aligner and Bitslip** tab. Use this parameter for implementing CPRI (Auto) protocol.	-
	continued...

Description	Impact
Added Faster Register mode for PCS TX and RX FIFO.	-
Changed the parameter **Enable Reconfiguration between Standard and Enhanced PCS** to **Enable Datapath and Interface Reconfiguration**.	-
Changed the **one-time** option for CTLE and DFE adaptation mode to **Triggered** mode.	-
Removed **Enable tx_enh_fifo_cnt port** and **Enable rx_enh_fifo_cnt port** parameters from the IP **Parameter Editor**.	-
Removed the parameter **Device Speed Grade**selection.	-
Removed 62.5, 125, 200, and 250 values for PPM detector threshold.	-
Enhanced user warnings and information messages.	-
Added the following presets: • 3G SDI NTSC • 3G SDI PAL • HD SDI NTSC • HD SDI PAL • Low Latency GT • SAS Gen1 • SAS Gen1.1 • SAS Gen2 • SATA Gen1 • SATA Gen2 • SATA Gen3 • SFI-S 64:64 4x11.3Gbps • SONET/SDH OC-12 • SONET/SDH OC-48 • SONET/SDH OC-96 • Serial Rapid IO 1.25Gbps	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.5 Arria 10 Transceiver Native PHY IP Core v13.1 Revision History

Table 6. v13.1 Arria 10 Edition

Description	Impact
Initial release for Arria 10 devices.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores