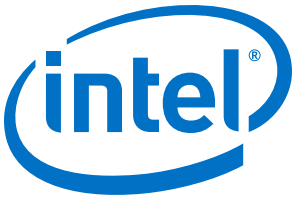

Arria 10 FPLL IP Core Release Notes

RN-1131
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Contents

1 Arria 10 FPLL IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Quartus Prime Design Suite Update Release Notes*.

Related Links

Quartus Prime Design Suite Update Release Notes

1.1 Arria 10 FPLL IP Core Revision History v16.1 Revision History

Table 1. v16.1 October 2016

Description	Impact
Issue: During Arria 10 FPLL reconfiguration, `pll_locked` signal can deassert indicating that FPLL loses lock to reference clock. The behavior is limited to the condition when reference clock `pll_refclk<n>` changes at the same time with FPLL reconfiguration. **Workaround:** No. **Resolution:** The simulation model in Quartus Prime 16.1 is updated to fix the behaviour.	Simulation only. Silicon is not affected.

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Intel FPGA IP Cores

1.2 Arria 10 FPLL IP Core Revision History v15.1 Revision History

Table 2. v15.1 Novembver 2015

Description	Impact
Changed the "Enable cascade clock input port" parameter name to "Enable ATX to FPLL cascade clock input port."	—
Issue: ACDS 15.1 introduces a necessary fix for Arria 10 transceiver designs. This fix introduces a change that affects post-fit simulation for designs containing Arria 10 Transceiver Native PHY, Arria 10 Transceiver ATX PLL, Arria 10 Transceiver CMU PLL, and Arria 10 fPLL IP cores. `pll_powerdown` is not connected for HSSI PLL IPs. **Workaround:** Users requiring post-fit simulation of the transceiver PLLs in ACDS 15.1 need to disable the "Transceiver Reset Sequencer" for their design to produce a post-fit simulation netlist. However, this cannot and should not be used to produce the final bitstream for hardware. Hardware requires the "Transceiver Reset Sequencer" to be enabled.	`pll_powerdown` inputs to the Arria 10 Transceiver ATX PLL, Arria 10 Transceiver CMU PLL, and Arria 10 fPLL IP cores for Quartus Prime synthesis. As a result, the resulting generated post-fit simulation will not have a reset input connection for the PLL and post-fit simulation will likely fail.

continued...

Description	Impact
To disable the "Transceiver Reset Sequencer" in the Quartus Prime software, add the following QSF to the Quartus Settings File for the project: `set_global_assignment -name VERILOG_MACRO "ALTERA_XCVR_A10_ENABLE_ANALOG_RESETS=1"` This will completely disable the reset sequencer in the design and restore the old behavior. This method does not allow post-fit simulation of the "Transceiver Reset Sequencer" logic. **Resolution:** A modification to the PLL simulation models is planned for a subsequent release of ACDS 15.1 to remove the reset requirement.	

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.3 Arria 10 FPLL IP Core Revision History v15.0 Revision History

Table 3. v15.0 May 2015

Description	Impact
Changed the following GUI warning: Warning (10858): Verilog HDL warning at altera_xcvr_fpll_a10.sv(487): object pll_extfb_wire used but never assigned. This compile warning resulted from a dangling net left behind when the CGB master was not generated (enabled). Tied off the `pll_extfb_wire` signal when the CGB master is not generated to drive it.	-
Added an **Advanced Parameters** tab that displays the following values: • C counters (0 to 3) • L, M and N counters • K fractional division • VCO frequency	-
Truncated the return vco frequency (MHz) to six digits after the decimal point.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.4 Arria 10 FPLL IP Core Revision History v14.1 Revision History

Table 4. v14.1 December 2014

Description	Impact
Changed the default FPLL Mode to Transceiver TX PLL.	-
FPLL does not allow the bandwidth setting of "high" in fractional mode.	
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or

continued...

Description	Impact
	v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.5 Arria 10 FPLL IP Core Revision History v14.0 Revision History

Table 5. v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the **Dynamic Reconfiguration** tab.	-
Changed the FPLL Parameter Editor graphic user interface (GUI) to show the available FPLL modes. You can use the FPLL in the following three modes: • Core • Cascade Source • Transceiver	-
Removed the option for automatic bandwidth setting. The following bandwidth settings are available: • Low • Medium • High	-
Enhanced user warnings and information messages.	-
The fPLL IP in 13.1 Arria 10 edition, allowed simultaneous selection of FPLL to be used in core and transceiver PLL modes. However, in the FPLL IP in 14.0 Arria 10 edition, only one mode (transceiver PLL or core PLL) can be selected at a time. If you have selected both (transceiver PLL and core PLL) modes in 13.1 Arria 10 edition, then FPLL IP will fail automatic upgrade for 14.0 Arria 10 edition. In this case, you will have to manually upgrade the FPLL IP after selecting one legal FPLL usage mode.	-
The **Master Clock Generation Block** tab in IP Parameter Editor is not visible when "Core" is selected as the FPLL mode. The **Master Clock Generation Block** tab appears only when "Transceiver" is selected as the FPLL mode.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.6 Arria 10 FPLL IP Core Revision History v13.1 Revision History

Table 6. v13.1 Arria 10 Edition

Description	Impact
Initial release for Arria 10 devices.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores