

10-Gbps Ethernet (10GbE) MAC IP Core Release Notes

2016.05.02

RN-1121



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If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Altera Complete Design Suite Update Release Notes*.

Related Information

[Altera Complete Design Suite Update Release Notes](#)

10-Gbps Ethernet (10GbE) MAC v15.1

Table 1: v15.1 November 2015

Description	Impact
Enhanced unidirectional feature to support user-triggered remote fault notification through the register bit.	—

Related Information

- [Introduction to Altera IP Cores](#)
- [10-Gbps Ethernet \(10GbE\) MAC MegaCore Function User Guide](#)
- [Errata for 10-Gbps Ethernet \(10GbE\) MAC MegaCore Function in the Knowledge Base](#)

10-Gbps Ethernet (10GbE) MAC v15.0

Table 2: v15.0 May 2015

Description	Impact
Added new TX and RX registers, <code>vlandet_dis</code> , in the frame decoder for the option to disable VLAN or stacked VLAN tag detection. To disable the detection of VLAN/SVLAN type frame (length type field = 0x8100), set the register to 1.	This new register is available when you upgrade the IP core to v15.0

Related Information

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10-Gbps Ethernet (10GbE) MAC v14.0

Table 3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added support for clause 66 of IEEE 802.3—synthesis option.	This change is optional. If you do not upgrade your IP core, it does not have this new feature.

Related Information

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10-Gbps Ethernet (10GbE) MAC v13.1

Table 4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • HardCopy IV GX • Stratix II GX 	-
Removed 1G/10GbE MAC and 10M-10GbE MAC with IEEE 1588v2 design examples from the directory.	-
The 10GbE MAC with 10GBASE-R PHY and IEEE 1588v2 configuration supports only Arria V GT device with speed grade 3_H3.	-
Increased the width for path delay interface signals such as <code>tx_path_delay_10g_data</code> (16 bits), <code>tx_path_delay_1g_data</code> (22 bits), <code>rx_path_delay_10g_data</code> (16 bits), and <code>rx_path_delay_1g_data</code> (22 bits)	-

Related Information

- [Introduction to Altera IP Cores](#)
- [10-Gbps Ethernet \(10GbE\) MAC MegaCore Function User Guide](#)
- [Errata for 10-Gbps Ethernet \(10GbE\) MAC MegaCore Function in the Knowledge Base](#)