# MAX II CPLD Features

View device ordering codes on **page 40**.

| | | MAX II CPLDs (3.3 V, 2.5 V, 1.8 V) | | | |
|---|---|---|---|---|---|
| | | **EPM240/Z** | **EPM570/Z** | **EPM1270** | **EPM2210** |
| **Density and Speed** | Equivalent macrocells[1] | 192 | 440 | 980 | 1,700 |
| | Pin-to-pin delay (ns) | 4.7, 7.5 | 5.4, 9.0 | 6.2 | 7.0 |
| **Architectural Features** | User flash memory (Kb) | 8 | | | |
| | Boundary-scan JTAG | ✓ | | | |
| | JTAG ISP | ✓ | | | |
| | Fast input registers | ✓ | | | |
| | Programmable register power-up | ✓ | | | |
| | JTAG translator | ✓ | | | |
| | Real-time ISP | ✓ | | | |
| **I/O Features** | MultiVolt I/Os (V) | 1.5, 1.8, 2.5, 3.3 | 1.5, 1.8, 2.5, 3.3 | 1.5, 1.8, 2.5, 3.3, 5.0[2] | 1.5, 1.8, 2.5, 3.3, 5.0[2] |
| | I/O power banks | 2 | 2 | 4 | 4 |
| | Maximum output enables | 80 | 160 | 212 | 272 |
| | LVTTL/LVCMOS | ✓ | | | |
| | 32 bit, 66 MHz PCI compliant | – | – | ✓[2] | ✓[2] |
| | Schmitt triggers | ✓ | | | |
| | Programmable slew rate | ✓ | | | |
| | Programmable pull-up resistors | ✓ | | | |
| | Programmable GND pins | ✓ | | | |
| | Open-drain outputs | ✓ | | | |
| | Bus hold | ✓ | | | |

Notes:

1. Typical equivalent macrocells.
2. An external resistor must be used for 5 V tolerance.