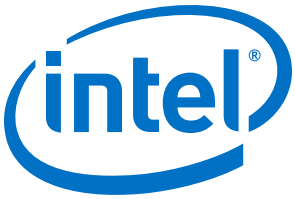

Nios® II Performance Benchmarks

DS-1066 | 2020.05.14
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Contents

1. Overview

This datasheet lists the performance and logic element (LE) usage for a typical implementation of a Nios® II soft processor and peripherals. Nios II processors are configurable and designed for implementation in Intel® FPGAs. The following Nios II processors cores were used for these benchmarks:(1)

- Nios II/f—The Nios II/f "fast" processor is designed for high performance and has the most configuration options, some of which are unavailable in the Nios II/e processor.
- Nios II/e—The Nios II/e "economy" processor is designed for the smallest possible logic size while still providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.

Note: Results may vary slightly depending on the version of the Intel Quartus® Prime software, the version of the Nios II processor, compiler version, target device and the configuration of the processor. Also, any changes to the system logic design might change the performance and LE usage. All results are generated from designs built using the Platform Designer tool.

The Dhrystone MIPS (DMIPS) reports were obtained using the Dhrystone 2.1 benchmark. You can download the Dhrystone 2.1 benchmark software with the **Fast Nios II Hardware Design Example** on the Intel FPGA website. For more information about the Dhrystone 2.1 benchmark software and the Fast design example, refer to the **readme.txt** file which is included in the design example page.

The CoreMark software can be registered and downloaded at *www.eembc.org*.

Note: The Nios II Classic and Nios II benchmark data are very similar. The Nios II processor was used to create the systems which gave the data values reported in this document. Please refer to the older versions of this document for values associated with the Classic cores.

The resource utilization results were generated using moderate Analysis, Synthesis and Fitter settings in the Quartus Prime software. These results represent typical results.

(1) The Nios II/s core is only available with the Nios II Classic soft processor.

Table 1. System Configuration for Nios II Performance Benchmarks

Benchmark	Nios II Processor	I-Cache	D-Cache	Other options	Peripherals
f_{max}	Nios II/f	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer
	Nios II/e	None	None	• JTAG debug module (default)	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer
Logic size	Nios II/f	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer • Avalon UART • SDRAM controller(3)
	Nios II/e	None	None	• JTAG debug module (default)	• 64 Kbytes On-chip RAM • Avalon Memory-Mapped pipeline Bridge • JTAG UART • Timer • Avalon UART • SDRAM controller(3)
DMIPS	Nios II/f at 100 MHz	4 Kbytes	2 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 128 Kbytes On-chip RAM • JTAG UART • Timer
	Nios II/e at 100 MHz	-	-	• JTAG debug module (default)	• 128 Kbytes On-chip RAM • JTAG UART • Timer
CoreMark(2)	Nios II/f at 100 MHz	32 Kbytes	32 Kbytes	• JTAG debug module (default) • Hardware multiplier	• 128 Kbytes On-chip RAM • JTAG UART • Timer
	Nios II/e at 100 MHz	-	-	• JTAG debug module (default)	• 128 Kbytes On-chip RAM • JTAG UART • Timer

Related Information

- Fast Nios II Hardware Design Example
- CoreMark Software Download

(2) This benchmark is compiled with the gcc -o3 switch for optimised performance.

(3) The RAM controller for the device is based on DDR3 SDRAM Controller with UniPHY. For Intel Cyclone® 10, Intel Arria® 10, Intel Stratix® 10, and Intel Agilex™ devices, the RAM controller is based on the respective device IP.

2. Nios II Performance Benchmarks

Table 2. f_{max} for Nios II Processor System (MHz)

Device Family	Device OPN	Nios II/f	Nios II/e	Results are generated using
Intel Agilex	AGFA014R24A2E2VR0	400	410	Intel Quartus Prime Pro Edition software version 20.1
Intel Stratix 10	1SG250LN3F43I2LG	300	320	Intel Quartus Prime Pro Edition software version 20.1
Stratix V	5SGXEA7N2F45C1	350	410	Intel Quartus Prime Standard Edition software version 19.1
Stratix IV	EP4S100G5H40I1	240	280	Intel Quartus Prime Standard Edition software version 19.1
Intel Arria 10	10AX115U3F45I2LG	290	340	Intel Quartus Prime Pro Edition software version 20.1
Arria V GZ	5AGZME7K2F40C3	280	360	Intel Quartus Prime Standard Edition software version 19.1
Arria V	5AGXFB5K4F40I3	200	260	Intel Quartus Prime Standard Edition software version 19.1
Intel Cyclone 10 GX	10CX220YF780E5G	280	330	Intel Quartus Prime Pro Edition software version 20.1
Intel Cyclone 10 LP	10CL120YF780I7G	140	160	Intel Quartus Prime Standard Edition software version 19.1
Cyclone V	5CGXFC7D6F31C6	170	210	Intel Quartus Prime Standard Edition software version 19.1
Cyclone IV	EP4CGX30CF19C6	160	170	Intel Quartus Prime Standard Edition software version 19.1
Intel MAX® 10	10M50DAF484C6GES	160	160	Intel Quartus Prime Standard Edition software version 19.1

Table 3. Typical Logic Size for Nios II Processor Cores and Peripherals

Device Family	Processor Core / Peripheral							Results are generated using
	Nios II/f	Nios II/e	Nios II JTAG debug module	Avalon UART	JTAG UART	SDRAM Controller[4]	Timer	
Intel Agilex	1002	596	149	57	71	5999	77	Intel Quartus Prime Pro Edition software version 20.1
Intel Stratix 10 (ALM)	1006	414	148	58	70	4429	76	Intel Quartus Prime Pro Edition software version 20.1
Stratix V (ALM)	697	296	129	62	56	2635	68	Intel Quartus Prime Standard Edition software version 19.1
Stratix IV (ALUT)	1073	527	169	95	112	3809	92	Intel Quartus Prime Standard Edition software version 19.1
Intel Arria 10 (ALM)	803	322	114	55	60	3973	60	Intel Quartus Prime Pro Edition software version 20.1
Arria V GZ (ALM)	706	290	125	55	56	2632	54	Intel Quartus Prime Standard Edition software version 19.1
Arria V (ALM)	835	310	126	56	56	2470	55	Intel Quartus Prime Standard Edition software version 19.1
Intel Cyclone 10 GX (ALM)	847	346	116	56	60	2291	55	Intel Quartus Prime Pro Edition software version 20.1
Intel Cyclone 10 LP (LE)	2326	838	464	141	163	435	148	Intel Quartus Prime Standard Edition software version 19.1
Cyclone V (ALM)	848	305	127	56	57	2473	56	Intel Quartus Prime Standard Edition software version 19.1
Cyclone IV GX (ALUT)	2221	772	352	143	160	424	138	Intel Quartus Prime Standard Edition software version 19.1
Intel MAX 10 (LE)	2211	790	364	136	157	4671	139	Intel Quartus Prime Standard Edition software version 19.1

Table 4. Nios II Processor Architecture Performance

Performance Metric	Nios II/f	Nios II/e
DMIPS/MHz Ratio	0.753	0.107
CoreMark	229.148	19.234

(4) The RAM controller for the device is based on DDR3 SDRAM Controller with UniPHY. For Intel Cyclone 10, Intel Arria 10, Intel Stratix 10, and Intel Agilex devices, the RAM controller is based on the respective device IP.

Related Information

- AN-440: Accelerating Nios II Networking Applications
  For more information about the Nios II networking applications performance.
- Nios II Custom Instruction User Guide
  For more information about the Nios II floating-point custom instruction performance.
- Embedded Design Handbook
  For more information about the Nios II Configuration and Booting Solutions.

3. Document Revision History for Nios II Performance Benchmarks

Document Version	Changes
2020.05.14	• Updated for Intel Quartus Prime Pro Edition software version 20.1 and Intel Quartus Prime Standard Edition software version 19.1. • Added results for Intel Agilex device.
2018.10.15	• Updated for Intel Quartus Prime 18.1 version.
2017.12.18	• Updated for Intel Quartus Prime 17.1 version. • Added the Intel Cyclone 10 GX, and Intel Stratix 10 results.
2017.06.12	• Updated for Intel Quartus Prime 17.0 version. • Added the Intel Cyclone 10 LP results.
2016.06.24	• Updated for Intel Quartus Prime 16.0 version. • Added the Cyclone IV results.
2015.12.16	• Updated for Intel Quartus Prime 15.1 version. • Added the Intel Arria 10 and CoreMark results.