Altera Low Latency Ethernet 10G MAC IP Core Migration Guidelines

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Altera offers two Ethernet MAC IP cores that can support up to 10 Gbps speed mode—10-Gbps Ethernet (10GbE) Media Access Controller (MAC) IP core and Low Latency Ethernet 10G MAC IP cores. The Low Latency Ethernet 10G MAC IP core is an enhanced version of the 10GbE MAC IP core and it provides lower resources and lower latency with an improved MAC functionality.

Existing users of the 10GbE MAC IP core can migrate to the Low Latency Ethernet 10G MAC IP core with minimal modifications on the system. However, it is important for you to understand the differences between these two IP cores before proceeding with the migration. This document describes the differences of both the MAC IP cores and provides the migration steps from 10GbE MAC IP core to Low Latency Ethernet 10G MAC IP core.

As a summary, there are multiple major differences between 10GbE MAC IP core and Low Latency Ethernet 10G MAC IP.

Table 1: Summary of Low Latency Ethernet 10GbE MAC IP core vs 10Gbps Ethernet MAC IP

Table shows the summary for all the differences between these two IP cores for quick reference.

Features	Low Latency 10G Ethernet MAC IP core	10GbE MAC IP core
Supported Device	Arria 10, Arria V GZ, Stratix V	Cyclone, Arria, and Stratix devices except Arria 10 (1)
MAC Latency (TX + RX)	• 60.8 ns (MAC with 10Gbps) • 356.8 ns (MAC with 1Gbps) • 2968 ns (MAC with 100 Mbps) • 29168 ns (MAC with 10Mbps)	• 140.8 ns (MAC with 10 Gbps) • 422.4 ns (MAC with 1 Gbps) • 3128 ns (MAC with 100 Mbps) • 29968 ns (MAC with 10 Mbps)
Avalon Streaming (Avalon-ST) Interface Data width	32-bit, 64-bit	64-bit
XGMII Interface Data width	32-bit, 64-bit	64-bit

(1) Device variant and Quartus II version dependent. Refer to the 10-Gbps Ethernet MAC IP Core User Guide for more information.

Features	Low Latency 10G Ethernet MAC IP core	10GbE MAC IP core
Register mapping	• Starting address 0x0000 • Backward compatible with 10GbE Ethernet IP with 64-bit Avalon-MM adapter	Starting address 0x000
ECC detection and correction	Available	Not Available

Related Information

- **10-Gbps Ethernet MAC MegaCore Function User Guide**
- **Low Latency Ethernet 10G MAC User Guide**
- **Scalable Low Latency Ethernet 10G MAC using Arria 10 1G/10G PHY Design Example**
- **Scalable 10G Ethernet MAC using 1G/10G PHY Design Example**

Differences between 10GbE MAC IP Core and Low Latency Ethernet 10G MAC IP Core

Table below shows the general features supported by both the MAC IP cores. For full list of supported features, refer to its respective user guides.

Table 2: Features of the 10GbE MAC IP core and Low Latency Ethernet 10G MAC IP

Features	Low Latency Ethernet 10G MAC IP Core	10GbE MAC IP core
Multispeed operation (10M/100M/1G/10Gbps)	Yes	Yes
64-bits Avalon-Streaming (Avalon-ST) interface	Yes	Yes
32-bits Avalon-ST interface	Yes	—
64-bits XGMII PHY interface	Yes	Yes
32-bits XGMII PHY interface	Yes	—
GMII and MII PHY interface	Yes	Yes
Optional IEEE 1588v2 features	Yes	Yes
Optional statistic collections for transmit and receive datapaths	Yes	Yes
Optional ECC correction and detection	Yes	—
Compliant to IEEE 802.3 – 2008 specification	Yes	Yes

Two new additional features are available only in the Low Latency Ethernet 10G MAC IP core:

- 32-bits Avalon-ST interface and 32-bit XGMII PHY interface for reduced pin count.
- ECC correction and detection for all internal RAMs that reside in the MAC. This is to provide status on single bit data correction and multi bit error data detection in the RAM that is impacted by electrical or magnetic interference.

Architecture Overview

To support seamless migration from 10GbE MAC IP core to Low Latency Ethernet 10G MAC IP core, there are three additional modules in the design.

These three modules are:

- 64-bit Avalon-ST adapter for both TX and RX datapaths
- 64-bit Avalon-MM adapter
- 64-bit XGMII adapter for both TX and RX datapaths

The Avalon-ST adapter converts 32-bit datapath from the MAC to 64-bit datapath to the user interface while the Avalon-MM adapter converts the register mapping of the Low Latency Ethernet 10G MAC IP core to the 10GbE MAC IP core register mapping. This register mapping conversion enables existing users of the 10GbE MAC IP core to migrate to the Low Latency Ethernet 10G MAC IP core without any software modification.

Figure 1: Multispeed 10M/100M/1G/10GbE 10GbE MAC IP Core Block Diagram

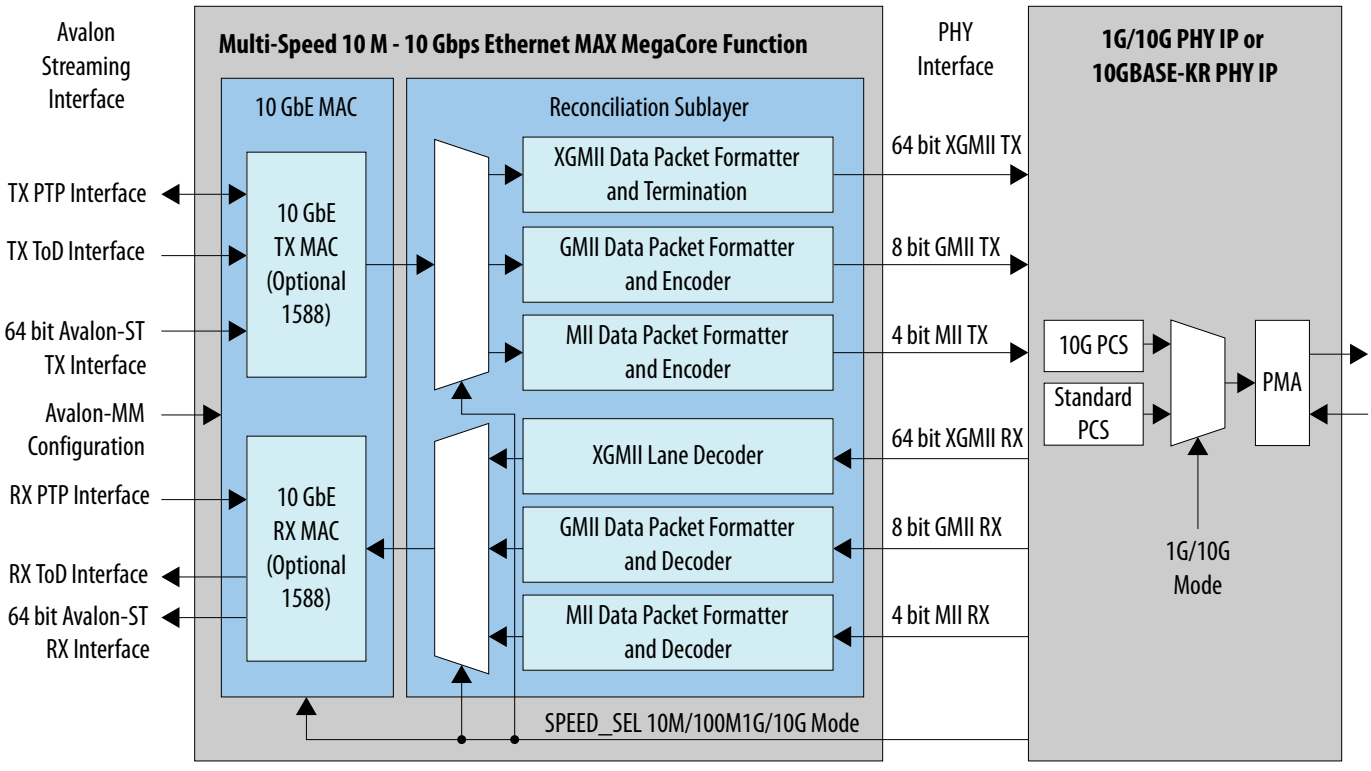
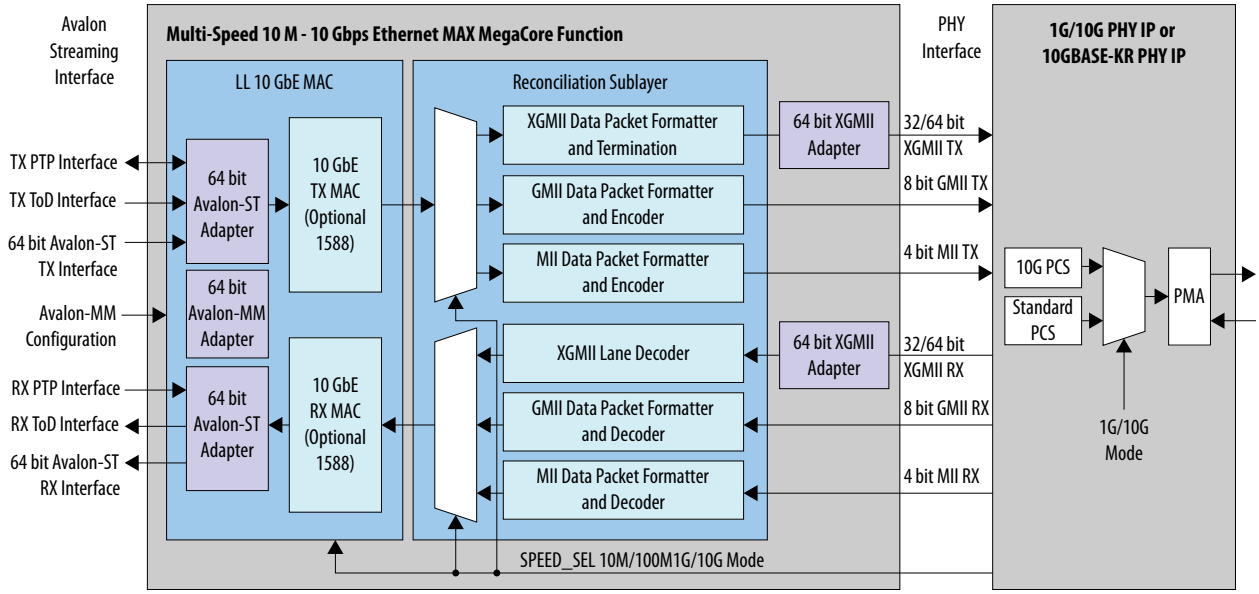


Figure 2: Multispeed 10M/100M/1G/10GbE Low Latency Ethernet 10G MAC IP Core Block Diagram



Clock and Reset Scheme

To support 32-bit data bus width for user interface and 32-bit XGMII data bus width for PHY interface, the transmit and receive clock for the Low Latency Ethernet 10G MAC IP core is increased from 156.25 MHz to 312.5 MHz.

However, you are required to supply 156.25 MHz of transmit and receive clock to the Low Latency Ethernet 10G MAC when the 64-bit Avalon-ST adapters, Avalon-MM adapter, and 64-bit XGMII adapters are enabled in the IP core.

The Low Latency Ethernet 10G MAC IP core provides reset signals for the TX datapath, RX datapath, and register configuration path. The reset signal for TX datapath resets both the 312.5 MHz and 156.25 MHz clock domains. The same applies for the RX datapath. Refer to the Low Latency Ethernet 10G MAC IP user guide for more description on the reset signals for this IP core.

Figure 3: Clock and Reset Scheme of 10GbE MAC IP Core Connected to 10GBASE-KR PHY IP Core

This figure shows an example of the clock and reset scheme of the 10-Gbps Ethernet MAC IP core connected to the 10GBASE-KR PHY IP core.

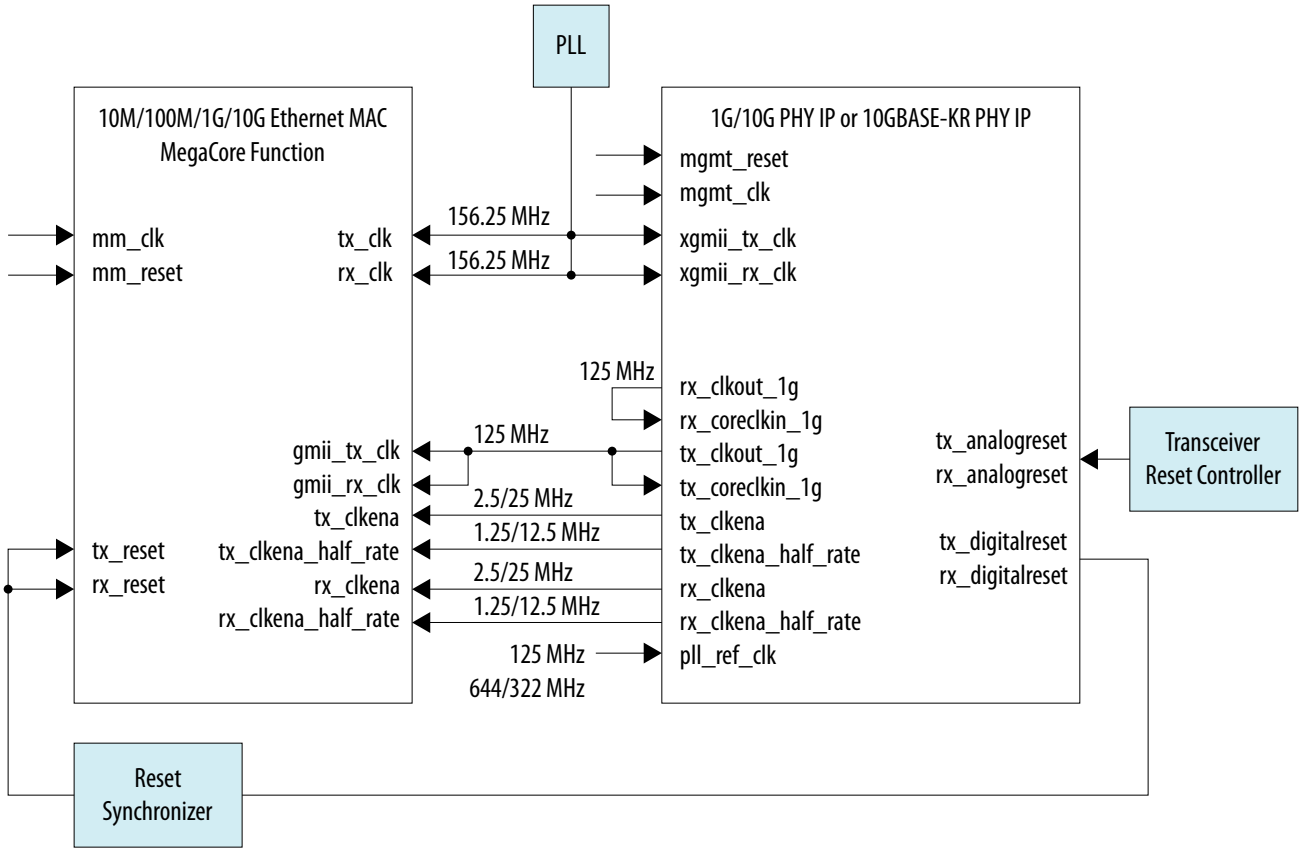


Figure 4: Clock and Reset Scheme of Low Latency Ethernet 10G MAC Connected to Altera 10GBASE-KR PHY IP Core for Stratix V and Arria V Devices

This figure shows an example of the clock and reset scheme of the Low Latency Ethernet 10G MAC IP core connected to the 10GBASE-KR PHY IP core with all adapters enabled in the Stratix V or Arria V devices. Additional clock signals are highlighted in blue.

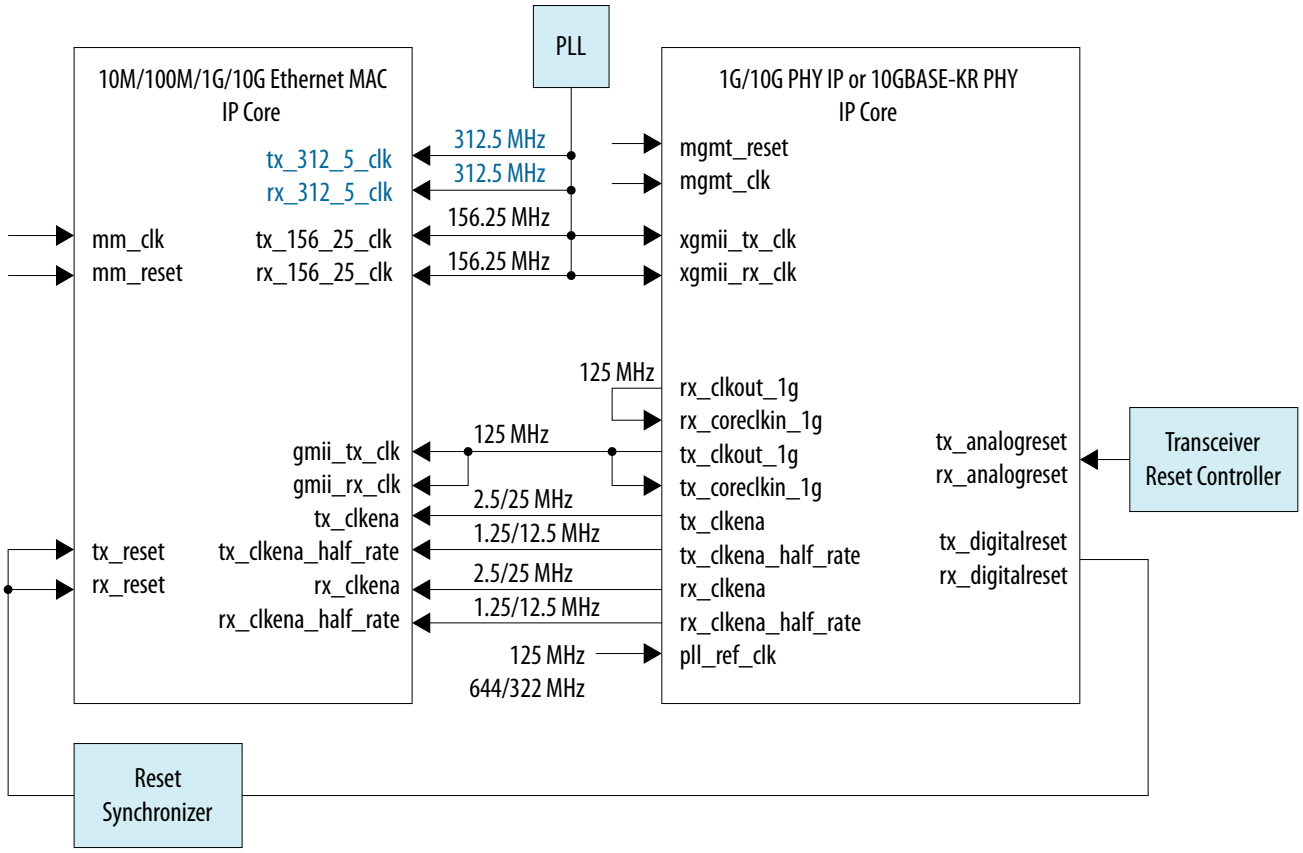
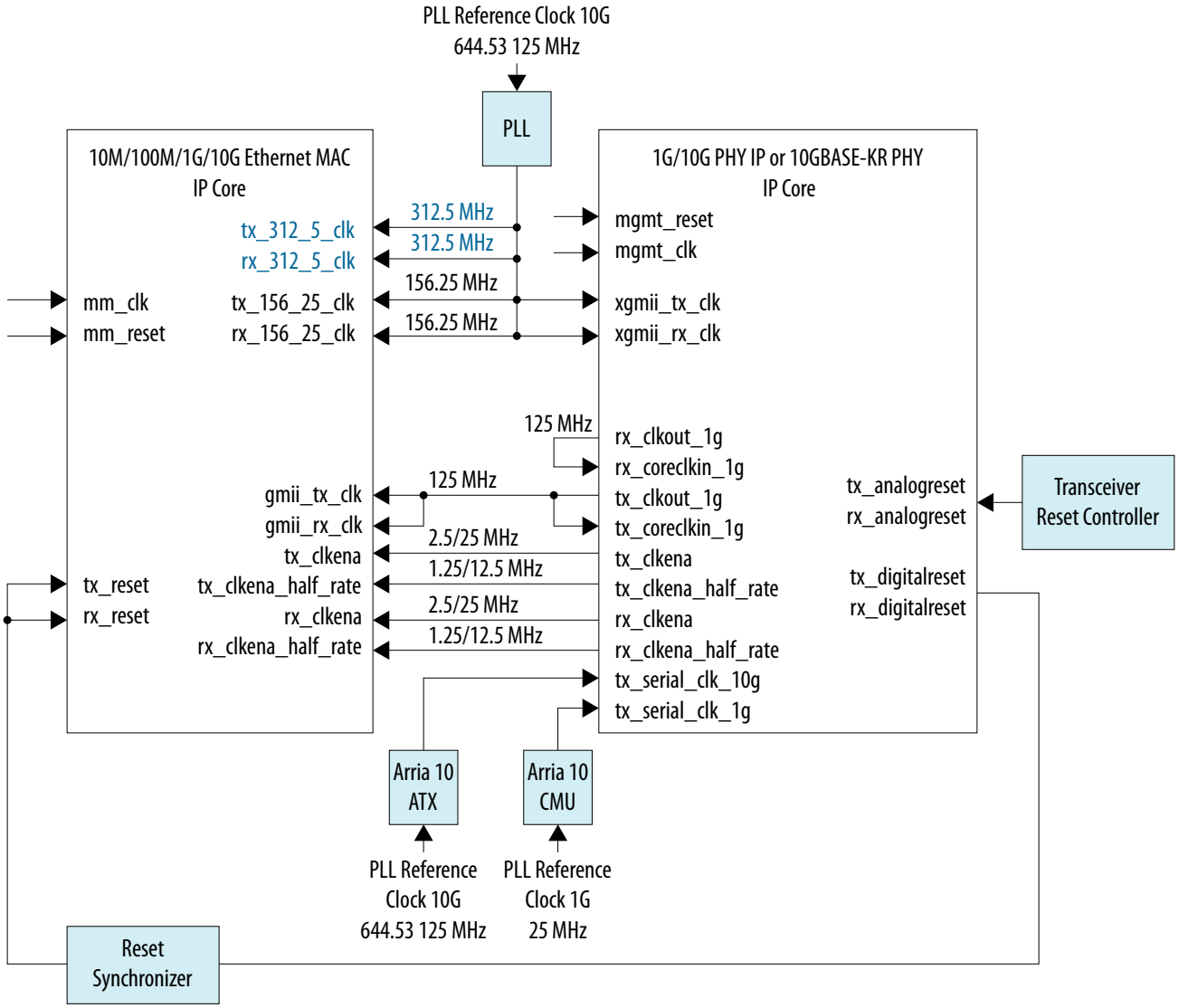


Figure 5: Clock and Reset Scheme of Low Latency Ethernet 10G MAC IP Core Connected to Altera 10GBASE-KR PHY IP Core for Arria 10 Devices

This figure shows an example of the clock and reset scheme of the Low Latency Ethernet 10G MAC IP core connected to the 10GBASE-KR PHY IP core with all adapters enabled in the Arria 10 device. Additional clock signals are highlighted in blue.



Interface Signals

There are several differences on the interface signals between 10GbE MAC IP core and Low Latency Ethernet 10G MAC IP core.

If the Low Latency Ethernet 10G MAC IP core with 64-bit Avalon-ST adapter, 64-bit Avalon-MM adapter, and 64-bit XGMII adapters are enabled, you may observe these additional signals in the IP core:

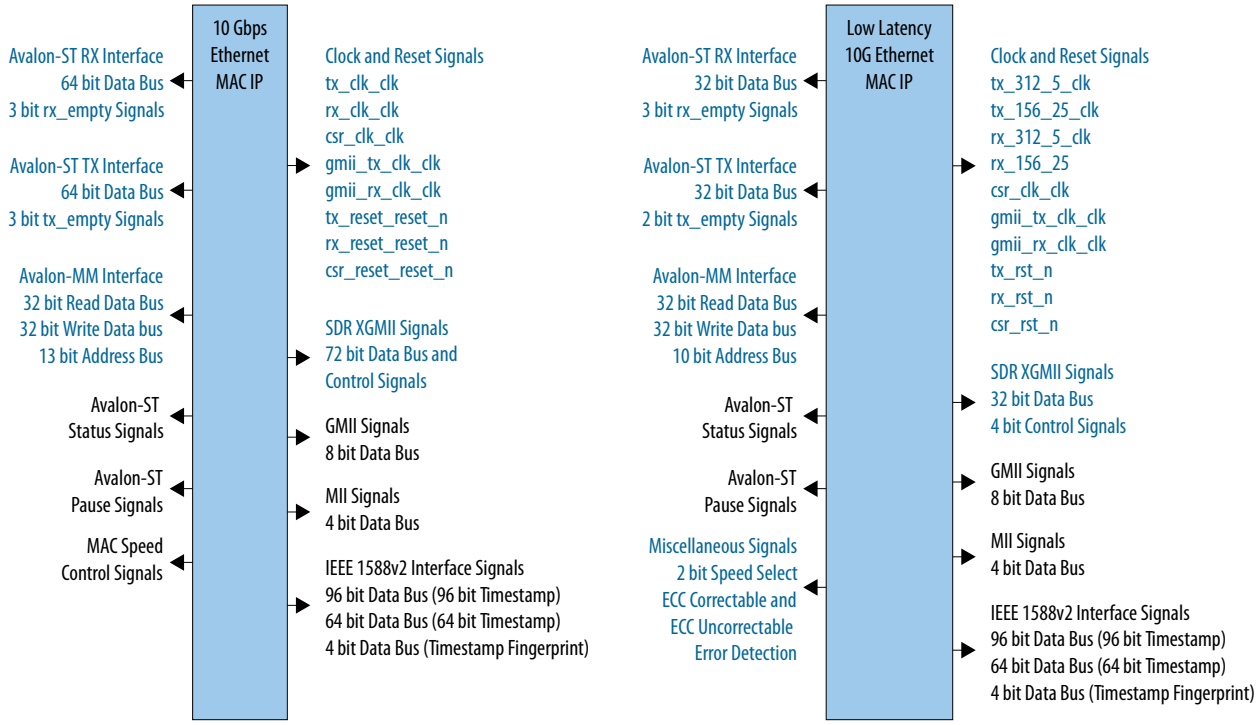
- tx_312_5_clk
- rx_312_5_clk
- ecc_err_det_corr
- ecc_err_det_uncorr

For the Low Latency Ethernet 10G MAC IP core instantiation without enabling any adapters, you may observe these signal names in the IP core:

- tx_312_5_clk
- rx_312_5_clk
- ecc_err_det_corr
- ecc_err_det_uncorr
- 10-bit csr_address
- 32-bit Avalon_st_tx_data
- 2-bit Avalon_st_tx_empty
- 32-bit Avalon_st_rx_data
- 2-bit Avalon_st_rx_empty
- 32-bit xgmii_tx_data
- 4-bit xgmii_tx_control
- 32-bit xgmii_rx_data
- 4-bit xgmii_rx_control

Figure 6: Interface Signal Differences for Low Latency Ethernet 10G MAC IP and 10GbE MAC IP core

This figure shows the interface signal differences between the 10GbE MAC IP core and Low Latency Ethernet 10G MAC IP core. The differences between these two IP cores are highlighted in blue.

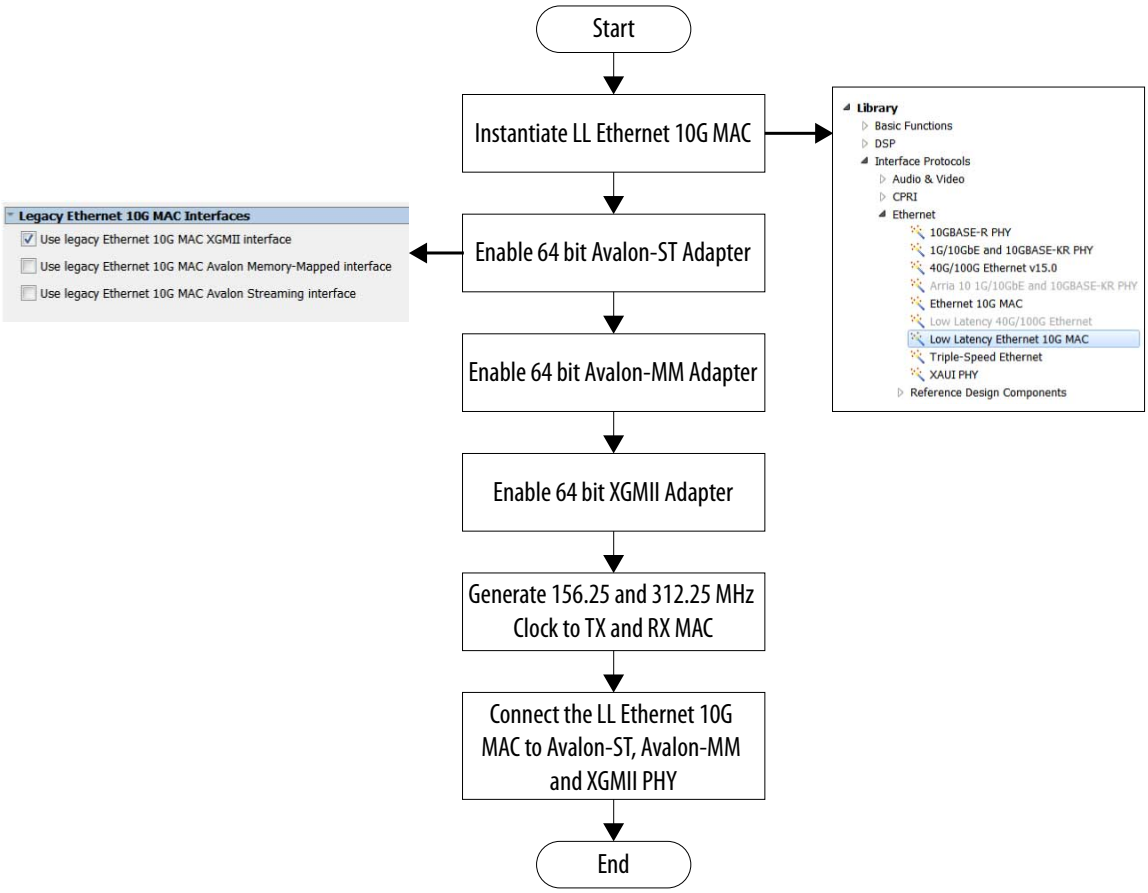


Migration Flow

The Low Latency Ethernet 10G MAC IP provides adapters which allow existing users of 10GbE MAC IP core to migrate to Low Latency Ethernet 10G MAC IP with minimal modifications to the system design.

Altera recommends that you follow this migration flow.

Figure 7: Recommended Migration Flow for Low Latency Ethernet 10G MAC IP Core



Instantiating Low Latency Ethernet MAC IP Core

Follow these steps to instantiate the Low Latency Ethernet 10G MAC IP core to replace the existing 10GbE MAC IP core in your system design.

1. Select and instantiate the Low Latency Ethernet 10G MAC IP core from the MegaWizard Plug-In Manager or IP Catalog.
2. In the Low Latency Ethernet 10G MAC parameter editor, select the same MAC variant used in the existing 10GbE MAC IP core in the user system design.
3. In the Low Latency Ethernet 10G MAC parameter editor, turn on the following parameters to enable all the adapters in the MAC interface:
   - For Quartus II version 14.1 or before: Under 64-bit Ethernet MAC Interfaces, select **Use 64-bit Ethernet 10G MAC XGMII Interface** , **Use 64-bit Ethernet 10G MAC Avalon Memory-Mapped Interface** and **Use 64-bit Ethernet 10G MAC Avalon Streaming interface**.
   - For Quartus II version 15.0 onwards: Under Legacy Ethernet 10G MAC Interfaces, select **Use legacy Ethernet 10G MAC XGMII Interface** , **Use legacy Ethernet 10G MAC Avalon Memory-Mapped Interface** and **Use legacy Ethernet 10G MAC Avalon Streaming interface**.
4. Click **Finish** or **Generate** to generate all the necessary files to synthesize the IP core.

Generating 156.25 MHz and 312.5 MHz Clock

The core clock for Low Latency Ethernet 10G MAC uses 312.5 MHz clock. Therefore, you are required to provide an additional 312.5MHz clock source to the MAC.

1. Instantiate a separate 312.5 MHz clock from any existing PLL in the design.
2. Connect this clock source to `tx_312_5_clk` and `rx_312_5_clk` signals. Both clock signals can share the same clock source.

Connecting the Low Latency Ethernet 10G MAC to Avalon-ST, Avalon-MM, and XGMII PHY Interfaces

After generating the synthesis file for the Low Latency Ethernet 10G MAC IP core, you can replace the existing 10GbE MAC IP core synthesis file (<*user_specified_ip_filename*>**.v**) with the newly generated Low Latency Ethernet 10G MAC synthesis file. Due to the differences in the signal names between both cores, you must make sure these signals are connected correctly to the user and PHY interfaces.

Table 3: Differences in Signal Names for Low Latency Ethernet 10G MAC IP Core and 10GbE MAC IP Core

This table lists the signal names in the Low Latency Ethernet 10G MAC IP core with all 64-bit MAC interface adapters enabled and its corresponding signals in the 10GbE MAC IP core.

Low Latency Ethernet 10G MAC IP Signal Names	10GbE MAC IP Core Signal Names
csr_clk	csr_clk_clk
csr_rst_n	csr_reset_reset_n
tx_156_25_clk	tx_clk_clk
tx_rst_n	tx_reset_reset_n
rx_156_25_clk	rx_clk_clk
rx_rst_n	rx_reset_reset_n

AN 735 Document Revision History

Table 4: Document Revision History

Date	Version	Changes
May 2015	2015.05.04	Initial release.