White Paper

FPGA
RF Spectrum Monitoring

Wide Instantaneous Bandwidth Digital Receivers Revolutionize RF Spectrum Monitoring Architectures

RF spectrum monitoring system developer BANC3 in Princeton, NJ leverages Intel's FPGAs in combination with Analog Devices' high-speed ADCs to achieve 18 GHz of instantaneous bandwidth for a SWaP-C efficient digital receiver architecture that maximizes probability of intercept for use in monitoring today's most challenging RF signal environments.

Today's radio frequency (RF) environment is increasingly crowded and complex as both commercial and military systems exploit an ever-expanding amount of the spectrum with waveforms including pulsed, continuous wave (CW), spread spectrum, frequency agile, frequency modulated (FM), amplitude modulated (AM), and phase modulated (PM). The requirement to provide high probability of intercept (POI) systems that can rapidly and accurately detect and identify threats and/or signals of interest masked by signal clutter typical of population-dense urban areas necessitates the use of receiver architectures with wide instantaneous bandwidth (IBW), high dynamic range, immunity to measurement errors resulting from multiple simultaneous signals, significant digitization speeds, and real-time processing capable of signal detection and parameter extraction. To meet the challenge of evolving threats and agile waveforms including cognitive radio and cognitive radar, the signal detection and processing needs to be highly adaptable, reprogrammable, and flexible enough to meet changing mission priorities while providing a level of autonomy that eliminates the need for pre-programmed mission data files.

BANC3 is leading the way in the design, development, and production of RF spectrum monitoring systems with extremely wide IBW. Our system architecture focuses on RF and digital channelization coupled with parallel real-time processing in both the frequency and time domains to create a continuous stream of content rich data that accurately characterizes the RF spectrum. Our systems stand apart from the traditional narrow band systems using tuners swept over frequency by offering you an effective solution for detection of transient, short duration RF events by channelizing, digitizing, and processing the entire RF bandwidth continuously. Our system solutions can provide up to 18 GHz of IBW. When capturing every pulse with 100% POI is your mission … BANC3 has your RF spectrum monitoring solution.

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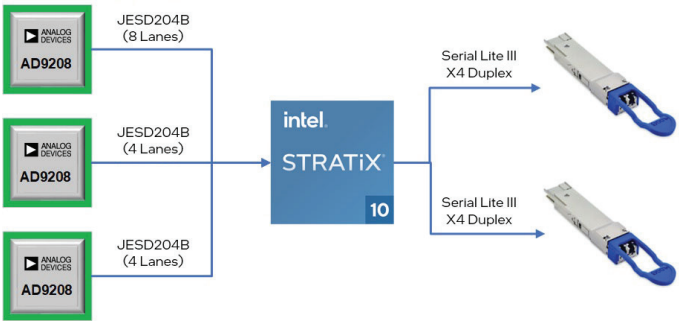
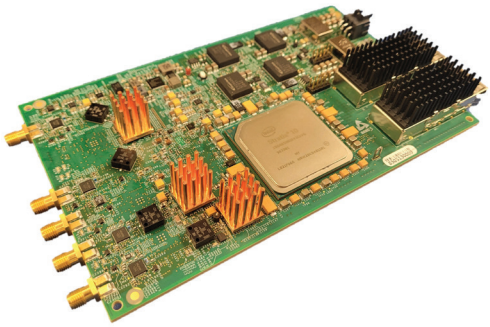
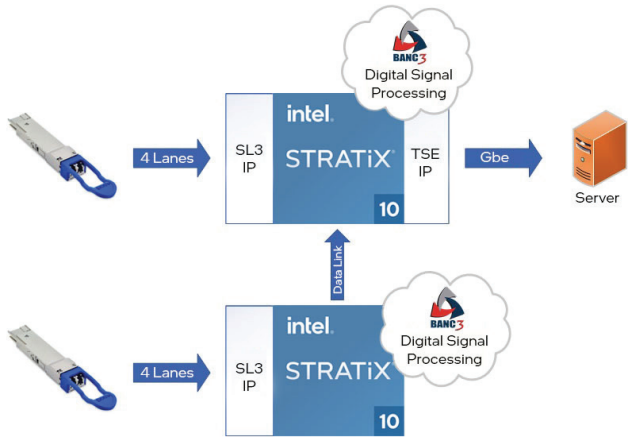
A recent opportunity in the aerospace/defense market focused on designing and manufacturing an RF spectrum monitoring system to support satellite payload launch operations. Our challenge was to instantaneously and continuously monitor 10 MHz – 18 GHz with sufficient accuracy and dynamic range to detect and report any RF signals that could potentially damage the sensors in the satellite payload. The system's front end would be located close to the launch site, where it would be exposed to extreme environmental shock and vibration conditions, while the digital signal processing would be performed in a receiver at a sheltered location 10 km away. A 100 Gb/s fiber optic network would transport the high-speed digital data from the launch site to the receiver site. Size, weight, power, and cost (SWaP-C) were important drivers for development and manufacturing. After an in-depth design effort, BANC3's team turned to Intel and Analog Devices to provide the critical components necessary to accomplish this challenging mission.

The RF front end uses the Analog Devices AD9208 high-speed analog-to-digital converter (ADC) to digitize and filter the signal. Key technical factors in this decision included the number of bits (14 bits) to maximize dynamic range, the sampling speed (3 GSPS) to maximize unambiguous bandwidth, the integrated digital filtering and digital downconverter (DDC) to support digital channelization and resampling of the RF channels. The Intel® Stratix® 10 FPGA collects and formats the JESD204B data from the ADC for transport over the fiber optic interface using Serial Lite III. The availability of Intel® FPGA intellectual property (IP) for these high-speed interfaces in conjunction with enough high-speed transceivers to support the 100 Gb/s fiber optic link were important discriminators. This hardware configuration provides flexibility and expansion supporting customization of the receiver architecture to meet new and changing requirements. The high-speed ADC card features four RF channels, 10 MHz external reference, variable gain amplifiers for input signal level adjustment, digitization rate up to 3 GSPS, and 100 Gb/s fiber optic interfaces. This design is implemented using three AD9208 ADCs and one Intel® Stratix® 10 FPGA.





The Receiver uses the Intel® Stratix® 10 FPGA to implement BANC3's proprietary digital signal processing algorithm known as the Hybrid Digital Receiver. This unique, real-time digital receiver architecture uses both a Real Time Spectrum Analyzer (RTSA) and Digital Instantaneous Frequency Measurement (DIFM) receivers in parallel. These pipelined receivers implemented in the Intel® Stratix® 10 FPGA ensure 100% of the digital data stream is processed continuously and without interruption. The RTSA provides you with max-hold and average spectra data while the DIFM provides Pulse Descriptor Word (PDW) data detailing frequency, amplitude, pulse width and time of arrival for every RF event including pulses down to 50 ns up to CW. The Intel® Stratix® 10 FPGA provides enough logic gates to replicate and scale the receiver pipelines for each channel, and the DSP Builder for Intel® FPGAs was used to optimize the fast Fourier transforms (FFTs) used in the RTSA pipeline, resulting in an FPGA logic reduction from 80% to under 50% with no impact to performance while easing timing closure. The Digital Receiver card features four channels, 100 Gb/s fiber optic interfaces, and triple speed ethernet interface using two Intel® Stratix® 10 FPGAs.



Throughout the development cycle, we used evaluation boards for the AD9208 and Intel® Stratix® 10 FPGA to test and analyze our designs on the bench. These evaluation platforms provided an affordable rapid prototyping capability, allowing us to develop our custom IP while gaining an in-depth understanding of the ADC performance and the Intel FPGA IP. We collected test data from our bench top prototype to support Preliminary and Critical design reviews, allowing us to quantify the effectiveness of the design. The use of these evaluation boards decreased our time to market while mitigating risk and ensuring a successful on-time delivery.

The first production run of the system was completed in Q2 2021 including more than 60 ADC cards and 60 Receiver cards. The system has successfully completed operational test and is currently being deployed. A second production run is planned for 2022.

Our latest development efforts are focused on extending the frequency range of the system to 50 GHz to meet the needs of the rapidly expanding 5G market and other defense-based millimeter wave radar systems. To accomplish the goal of nearly tripling the spectrum monitoring bandwidth while keeping the SWaP-C of the system at a practical level, we need to increase the IBW of the Hybrid Digital Receiver to 2.5 GHz using the Intel® Agilex™ FPGA and the Analog Devices AD9213 ADC. The AD9213 provides up to 10 GSPS using 12-bits per sample and the Intel® Agilex™ FPGA provides more than twice the throughput for our DSP application. The ADISimRF tool from Analog Devices has been an important design tool in evaluating the most effective RF front end design. Initial bench testing using evaluation boards from Intel and ADI has been successful and validates this design approach. This new receiver, emphasizing modularity and scalability, will be offered in 3U/6U VPX form factor to facilitate integration into existing tactical platforms. Receiver boards can be added as the frequency coverage requirements expand. We anticipate this new receiver system will be leveraged as special test equipment by commercial companies in support of 5G rollouts and the aerospace/defense community for tactical signals intelligence missions and multi-mode radar testing.

BANC3 is a small, woman-owned business in Princeton, NJ focused on developing technology solutions for today's most challenging RF data collection, analysis, and visualization missions for industry and defense customers. BANC3 has applied for a US patent for the Hybrid Digital Receiver and related digital signal processing technology.

Refer to http://banc3.com/RF-Systems for more details on our RF spectrum monitoring products.

Please contact rfsystems@banc3.com or 609-759-1900 x 208 to discuss your requirements.