

For Quartus® Prime 16.0.2, the following three steps for PCIe Gen1, Gen2, or Gen3 designs that target an Arria 10 ES2, ES3, or production device.

#### 1) Update QSF assignments

For Quartus Prime 16.0.2, update the Quartus Prime Settings File (.qsf) with the below settings for your PCIe design that targets an Arria® 10 ES2, ES3 or production device.

In the following, "\_N" represents the lane and you must have one set of these constraints per lane. For example if you have a two lane design, then you would have a set of constraints for lane 0 (N=0, e.g. txvr\_rx\_data\_0) and another set for lane 1 (N=1, e.g. txvr\_rx\_data\_1). Note that there are separate transceiver transmit and receive constraints.

```
set_instance_assignment -name XCVR_A10_RX_TERM_SEL R_R1 -to
<txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_A10_RX_ONE_STAGE_ENABLE
NON_S1_MODE -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_A10_RX_ADP_CTLE_ACGAIN_4S
RADP_CTLE_ACGAIN_4S_0 -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE
<xcvr_voltage> -to <txvr_rx_data_pin_N>
set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE
<xcvr_voltage> -to <txvr_tx_data_pin_N>
```

Use the value corresponding to the voltage supplied to the transceivers on your board. Note <xcvr\_voltage> = 0\_9V, 1\_0V or 1\_1V.

#### 2) Update PCIe Gen3 Preset (Gen1 and Gen2 do not require this step)

If you are upgrading your PCIe Gen3 IP from Quartus Prime 16.0 or earlier to Quartus Prime 16.0.1, follow the instructions below to update the Preset requested by the PCIe HIP.

Edit the Qsys file for your Arria 10 PCIe hard IP instantiation with a text editor and change the Gen3 preset parameter from

```
<parameter name="gen3_coeff_1_hwtcl" value="9" />
to
<parameter name="gen3_coeff_1_hwtcl" value="8" />
```

After making this change, open the Qsys file in Quartus Prime and regenerate the PCIe hard IP core with the updated parameter.

3) Compile your design with Quartus Prime.