Application of High-κ Gate Dielectrics and Metal Gate Electrodes to enable Silicon and Non-Silicon Logic Nanotechnology

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Abstract

High-κ gate dielectrics and metal gate electrodes are required for enabling continued equivalent gate oxide thickness scaling, and hence high performance, and for controlling gate oxide leakage for both future silicon and emerging non-silicon nanoelectronic transistors. In addition, high-κ gate dielectrics and metal gates are required for the successful demonstration of high performance logic transistors on high-mobility non-silicon substrates with high I_{ON}/I_{OFF} ratios.

Keywords: Nanotechnology; non-silicon; high-κ dielectric; metal gate; high-mobility

1. Introduction

Since the advent of the metal-oxide-semiconductor (MOS) system over 40 years ago, the SiO_2 gate oxide has been serving as the key enabling material in scaling silicon CMOS technology. However, continued SiO_2 gate oxide scaling is becoming exceedingly difficult since (a) the gate oxide leakage is increasing with decreasing SiO_2 thickness, and (b) SiO_2 is running out of atoms for further scaling. As Moore's law extends scaling and device performance into the 21st century, high-κ gate dielectrics and metal gate electrodes will be required for high-performance and low-power CMOS applications in the 45 nm node and beyond. In addition to facilitating standard Si CMOS transistors, the high-κ/metal gate combination is also important for enabling future high-performance and low gate-leakage emerging nanoelectronic transistors built upon non-silicon high-mobility materials, e.g. Ge, carbon nanotubes, and III-V substrates. The enabling of high-performance and low gate-leakage silicon and non-silicon transistor nanotechnology research via use of high-κ gate dielectrics and metal gate electrodes is discussed in this paper.

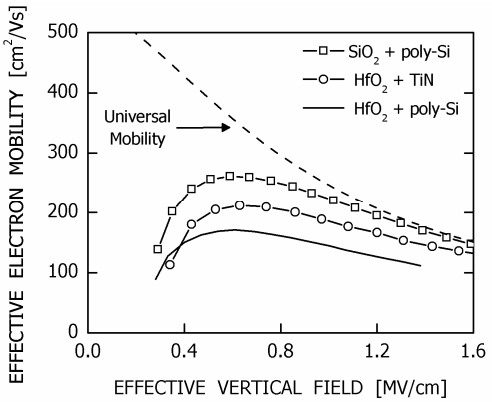

Fig.1 Effective electron mobility μ_{eff} as a function of effective vertical field E_{eff} comparing SiO_2/poly-Si, HfO_2/poly-Si, and HfO_2/TiN devices.

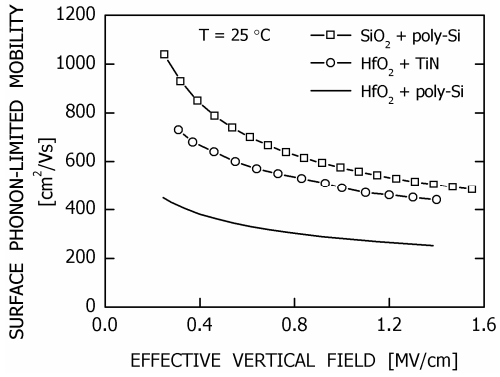

Fig.2 Surface phonon-limited mobility component at room temperature extracted from inverse modeling as a function of effective vertical field E_{eff}. The use of midgap TiN metal gate significantly improves channel mobility in high-κ gate dielectrics compared to conventional poly-Si gates.

2. High-κ/Metal-gate for Silicon Logic Nano-transistors

To date, Hf- and Zr-based high-κ gate dielectric materials are the most common studied by academia and industry. For the gate electrode, both poly-Si and various metals have been investigated in conjunction with such high-κ dielectrics. The choice between poly-Si or a metal as the gate electrode for the high-κ dielectric is crucial. The combination of a high-κ dielectric and a poly-Si gate is not suitable for high-performance logic applications since the resulting high-κ/poly-Si transistors have high threshold voltages and degraded channel mobility, shown in Figure 1, and hence poor drive current performance [1]. It has been proposed that the high threshold voltage is caused by Fermi level pinning at the poly-Si/high-κ dielectric interface [2] and that Fermi level pinning is most likely caused by defect formation at that very interface [3]. Furthermore, it has been demonstrated both experimentally [4] and theoretically [5] that surface phonon scattering in high-κ dielectrics is the primary cause of channel mobility degradation. Significantly, metal gate electrodes are effective for screening phonon scattering in the high-κ dielectric from coupling to the channel when under inversion conditions [4,5], as shown in Figure 2. This results in improved channel mobility as shown in Figure 1 [4].

The high-κ dielectric film attributes its high dielectric constant to its polarizable metal-oxygen bonds, which also give rise to low energy optical phonons. These phonons can be modeled as oscillating dipoles as shown in Figure 3. These oscillating dipoles couple strongly with the channel electrons when the gate plasma oscillations and the phonons in the high-κ dielectric are in resonance, as shown in Figure 3(a). This resonance occurs when the gate carrier density is $\sim 1 \times 10^{18}$ cm^{-3}, as is the case with standard doped poly-Si gate in depletion, and the corresponding gate plasmon energy falls within the dominant LO (longitudinal optical) and TO (transverse optical) energy modes of the high-κ dielectric [5]. This resonance condition leads to significant degradation of surface phonon-limited mobility. In the case of metal gate electrode, where the free carrier density exceeds 1×10^{20} cm^{-3}, the resonance condition is not satisfied [5], as shown in Figure 3(b). This weakens the carrier phonon coupling and leads to a recovery of the surface phonon-limited mobility.

Therefore, metal gates with "correct" work functions can be used to provide the right transistor threshold voltages, alleviate the mobility degradation problem, and enable high-performance high-κ/metal gate transistors with low gate dielectric leakages for future logic applications (Figure 4 illustrates work

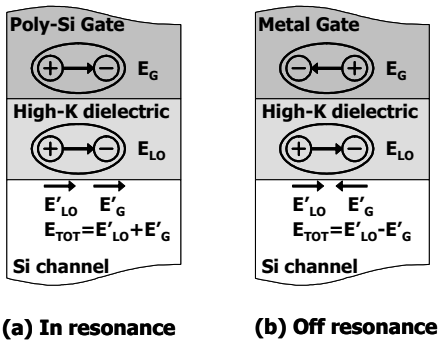

Fig.3 (a) Schematic of high-κ/poly-Si gate stack depicting gate plasma oscillations and high-κ phonons as electric dipoles in resonance, which results in degradation of surface phonon-limited mobility. (b) Schematic of high-κ/metal-gate stack depicting gate plasma oscillations and high-κ phonons as opposing electric dipoles, which reduce the coupling of high-κ phonons with carriers in the Si channel. In this case, the coupling is off-resonance and the surface phonon-limited mobility is recovered.

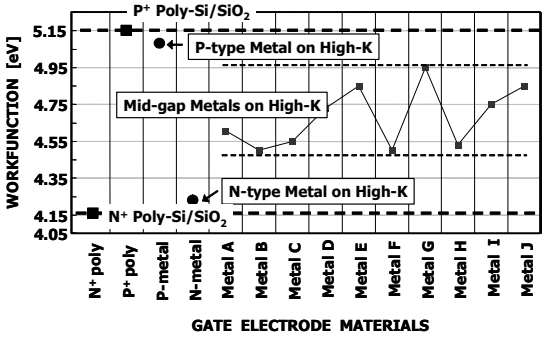

Fig.4 Workfunction of different gate electrode materials obtained from measured transistor flatband voltage.

functions for a variety of metals). For conventional planar CMOS applications on bulk silicon, a p^+ metal work function is needed for the PMOS transistor while an n^+ metal work function is required for the NMOS transistor, in order to satisfy the correct transistor threshold voltages. For fully-depleted SOI and other emerging nanoelectronic device applications, the use of midgap metals may be adequate to enable high performance CMOS transistors [6].

Recently, high-κ/metal gate CMOS transistors on bulk silicon with 1.0 nm equivalent oxide thickness have been demonstrated using an n^+ work function metal electrode for the NMOS transistor and a p^+ work function metal electrode for the PMOS transistor [1,4], as shown in Figures 5(a) and 5(b). The resulting high-κ/metal gate transistors exhibit good channel electron and hole mobility, correct n-channel and p-channel threshold voltages, and the expected high drive current performance for both the NMOS and PMOS transistors. The improvement in transistor drive currents is attributed to the scaling of electrical inversion gate oxide thickness and to an increase in channel inversion charge. This result shows experimentally that, unlike high-κ/poly-Si gate transistors that exhibit poor device performance,

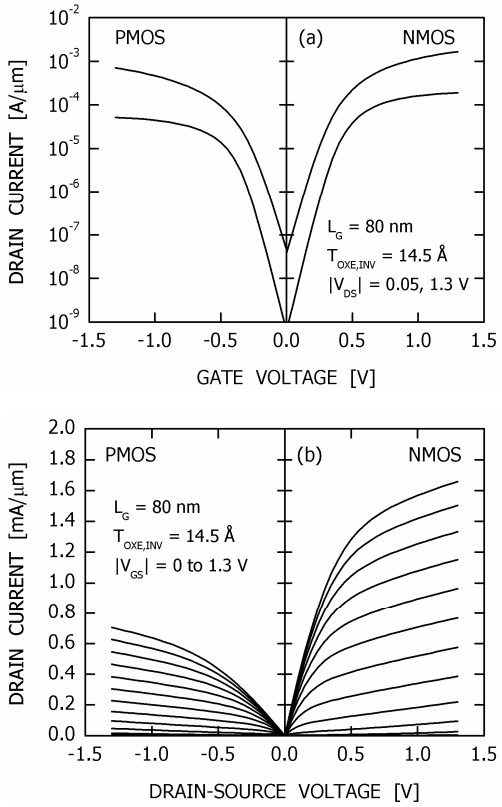

Fig.5 (a) I_{DS}–V_{GS} and (b) I_{DS}–V_{DS} characteristics of n-channel (right panel) and p-channel (left panel) high-κ/metal-gate MOSFETs. The transistors have physical gate length L_G = 80 nm and effective oxide thickness in inversion $T_{OXE,INV}$ = 14.5 Å.

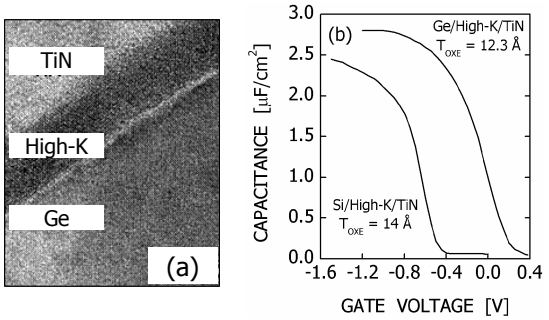

Fig.6 (a) TEM image of Ge/high-κ/TiN gate stack. (b) High frequency capacitance-voltage C–V curves of high-κ/TiN gate stacks on Ge and Si with effective oxide thickness T_{OXE} = 12.3 and 14 Å, respectively. The voltage shift of ~ 0.5 V between the two C–V curves reflects the bandgap difference of 0.45 eV between Si and Ge.

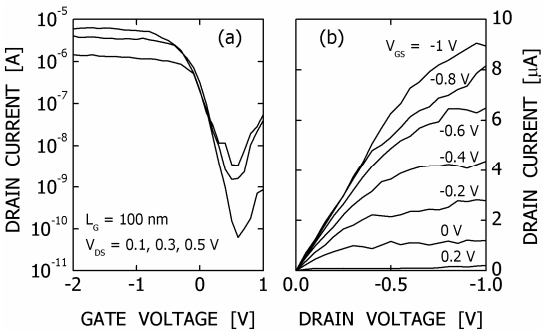

Fig.7 (a) I_{DS}–V_{GS} and (b) I_{DS}–V_{DS} characteristics of a CNTFET with gate length L_G = 100 nm and high-κ/metal-gate stack.

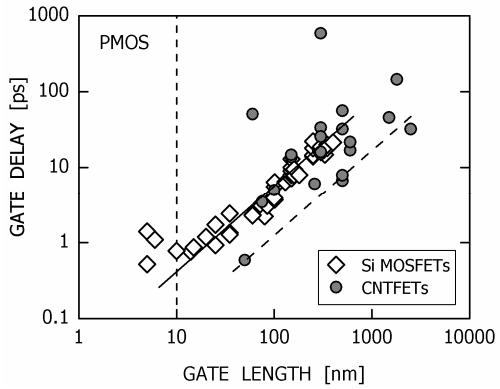

Fig.8 Gate delay (intrinsic device speed) CV/I versus transistor physical gate length L_G of PMOS devices.

very high-performance high-κ CMOS transistors can be achieved by employing metal gate electrodes on high-κ gate dielectrics.

3. High-κ/Metal-Gate for Emerging Nano-electronic Devices

In addition to facilitating standard Si CMOS transistors, the high-κ/metal gate combination is also important for enabling future high-performance and low gate-leakage emerging nanoelectronic transistors [13]. Recently, there has been much research interest in using non-silicon high-mobility materials, such as Ge [7], carbon nanotubes [8], and III-V quantum wells [9], as the device channel materials in high-performance transistors. For these emerging non-silicon nano-electronic devices, high-κ/metal gate is required for low equivalent oxide thickness for high performance and low gate oxide leakage. In addition, high-κ dielectrics have been demonstrated to be more compatible with some of these non-silicon substrates (e.g. Ge) versus their compatibility with conventional SiO_2. For example, while it is difficult to form good-quality SiO_2 on Ge, a high-quality high-κ dielectric can be formed on Ge with a minimal interfacial oxide layer and stable capacitance-voltage characteristics, as shown in Figures 6(a) and 6(b).

High-performance carbon nanotube field-effect transistors (CNTFETs) with very low gate dielectric leakage can also be fabricated with the use of high-κ/metal gate, as shown in Figure 7. The low gate dielectric leakage allows certain important source-drain leakage conduction mechanisms in CNTFETs, such as the ambipolar conduction mechanism, to be isolated and studied [8, 10, 13]. It has been shown that while CNTFETs exhibit high intrinsic speed (*CV/I*) performance, as shown in Figure 8, and low gate dielectric leakage, they suffer from a low I_{ON}/I_{OFF} ratio due to the presence of ambipolar leakage [8, 10, 11, 13], as illustrated in Figure 9. The determination of *CV/I* and I_{ON}/I_{OFF} of emerging nanoelectronic devices for logic applications are not discussed in this paper, but have been previously described in great detail in Refs. [8] and [10].

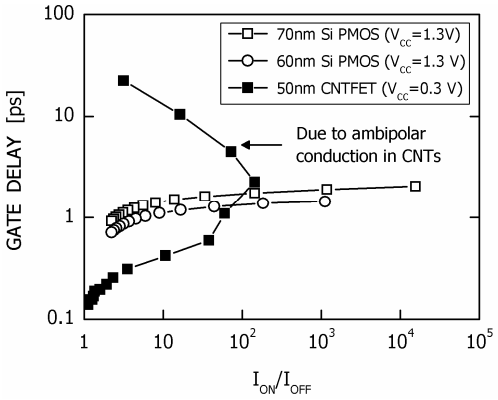

Fig.9 Gate delay (intrinsic device speed) CV/I versus on-to-off state current ratio I_{ON}/I_{OFF} of Si PMOS transistors with physical gate length L_G = 60 nm and 70nm at V_{CC} = 1.3 V, and a CNT PMOS transistor with L_G = 50 nm at V_{CC} = 0.3 V [11].

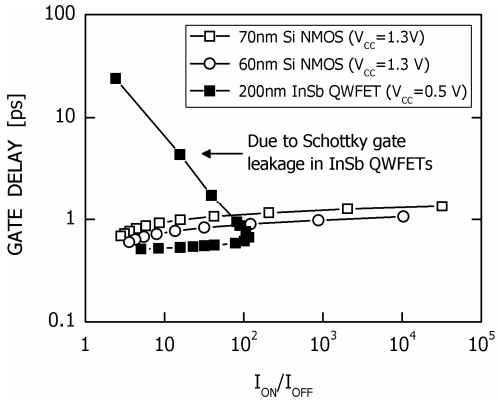

Fig.11 Gate delay (intrinsic device speed) CV/I versus on-to-off state current ratio I_{ON}/I_{OFF} of Si NMOS transistors with physical gate length L_G = 60 nm and 70nm at V_{CC} = 1.3 V, and an InSb n-type quantum-well FET (QWFET) with L_G = 200 nm at V_{CC} = 0.5 V [9].

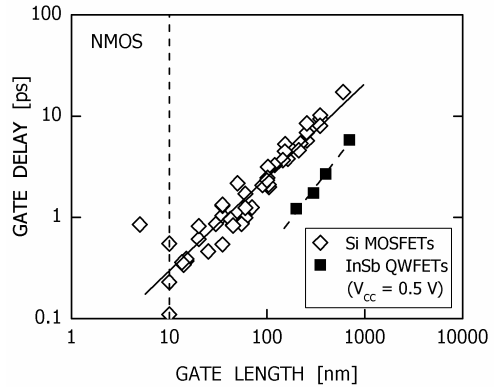

Fig.10 Gate delay (intrinsic device speed) CV/I versus transistor physical gate length L_G of NMOS devices [9].

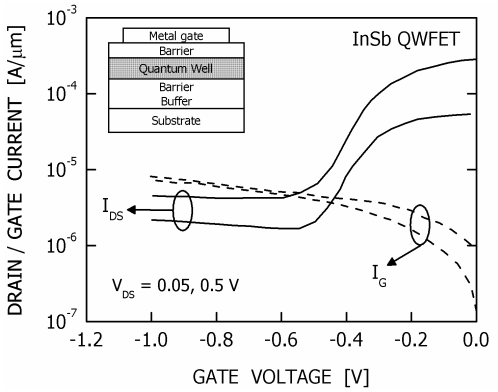

Fig.12 Drain current I_{DS} and gate leakage current I_G versus gate voltage V_{GS} of an InSb n-type quantum-well FET (QWFET) with gate length L_G = 200 nm [9]. Inset: Schematic of device layers in III-V material-based QWFETs with Schottky metal gates. I_G is the Schottky gate leakage due to the absence of gate dielectric [9].

The significance of high-κ dielectrics for emerging III-V transistors, such as InSb quantum-well transistors [9], is illustrated in Figures 10-12. Figure 10 demonstrates that when compared to standard Si devices, the InSb transistor shows much improved n-channel intrinsic speed (*CV/I*) due to higher channel mobility. However, like CNTs, the InSb transistor suffers from a low I_{ON}/I_{OFF} ratio, as shown in Figure 11. This phenomenon is a consequence of high gate leakage, exhibited in Figure 12, due to the low barrier height at the Schottky metal-semiconductor junction. The low barrier height arises from (a) Fermi-level pinning at the metal-semiconductor interface and (b) the use of a narrow-bandgap semiconductor. The use of a high-κ gate dielectric between the metal gate and the III-V device layers will eliminate such leakage and potentially improve the I_{ON}/I_{OFF} ratio.

4. Conclusions

For both future silicon and emerging non-silicon nanoelectronic transistors [12, 13], high-κ gate dielectrics and metal gate electrodes are required for enabling continued equivalent gate oxide thickness scaling, and hence high performance, and for controlling gate oxide leakage. In addition, high-κ gate dielectrics and metal gates are required for successful demonstration of high performance logic transistors on high-mobility non-silicon substrates with high I_{ON}/I_{OFF} ratios.

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